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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.     | CONFIRMATION NO.       |
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| 10/782,746  | 02/19/2004  | Andrew J. Peltoma    | 17310-296454            | 1661                   |
| 25764   | 7590        | 06/05/2007           |                         |                        |
| FAEGRE & BENSON LLP<br>PATENT DOCKETING<br>2200 WELLS FARGO CENTER<br>90 SOUTH SEVENTH STREET<br>MINNEAPOLIS, MN 55402-3901 |             |                      | EXAMINER<br>VAN, LUAN V |                        |
|   |             |                      | ART UNIT<br>1753        | PAPER NUMBER           |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/782,746

Applicant(s)

PELTOMA ET AL.

Examiner

Luan V. Van

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on April 26, 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-7, 9-13 and 23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-13 and 23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Response to Amendment***

Applicant's amendment of April 26, 2007 does not render the application allowable.

The amendment is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: Claims 1-7, 9-13 and 23 are amended to recite the limitations of "including forming masked portions of the conductive lead layer" and "wherein the first conductive material does not electroplate onto any unmasked portions of the conductive lead layer until the built up material reaches a thickness at which the conductive material contacts any unmasked portions of the conductive lead layer at the interconnect site". The disclosure does not provide a clear indication to support the limitations. Applicant is required to cancel the new matter in the reply to this Office Action.

***Status of Objections and Rejections***

All rejections from the previous office action are maintained.

New grounds of rejection under 35 U.S.C. 103(a) are necessitated by the amendments.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-7, 9-13 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1-7, 9-13 and 23 are amended to recite the limitations of "including forming masked portions of the conductive lead layer" and "wherein the first conductive material does not electroplate onto any unmasked portions of the conductive lead layer until the built up material reaches a thickness at which the conductive material contacts any unmasked portions of the conductive lead layer at the interconnect site". The disclosure does not provide a clear indication to support the limitations.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 6, 7, 9-11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowles et al. in view of Rinne et al.

Regarding claims 1, 7, 10, 11 and 23, Cowles et al. teach a method for forming an electrical interconnect on an integrated lead suspension of the type having a spring metal layer (stainless steel layer 302, figure 2), a conductive lead layer 306 (figure 2) and an insulating layer 304 (figure 2) separating portions of the spring metal and conductive lead layers, including: forming an aperture 300 (figure 2) through at least the insulating layer and the conductive lead layer; and filling the vias with plated solder or screen solder to connect a stainless steel layer to the copper layer (column 3 lines 63-67). The solder is applied through a mask as indicated in figure 2 and removing the mask after solder 308 is formed. The plated solder forms a plated interconnect having the physical structure of the material as plated prior to reflowing. It is noted that the amended limitation of "having the physical structure of the material as electroplated" does not exclude other processing steps, such as reflowing. In addition, Cowles et al.

teach forming a solder interconnect on the stainless steel spring layer to a height about equal to or greater than the surface of the copper lead layer (Fig. 2).

Cowles et al. differ from the instant claims in that the reference does not explicitly teach that the conductive material initially does not electroplate onto the unmasked portions of the conductive lead layer. Cowles et al. is also silent to electroplating the conductive material to a height about equal to or greater than the surface of the conductive lead layer, although Cowles et al. teach that the plated solder achieves this height after reflowing.

Rinne et al. teach electroplating an aperture or via in the insulating layer with a conductive material to the same thickness as the top surface layer (see Fig. 1F). In addition, Rinne et al. teach using a plating base layer 24 (Fig. 1) to provide a plating current for electroplating a conductive material, i.e. solder bumps 30.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. by electroplating on the base layer, i.e. the stainless steel layer of Cowles et al., as taught by Rinne et al., because it would build up an electroplated conductive material from the bottom of the aperture, thus preventing the formation of voids. It would have been obvious to one having ordinary skill in the art to have expected that the electroplated conductive material would form on the base layer first, because an electric current is applied to the base layer to effect the electrodeposition, while the conductive material does not initially electroplate onto the conductive lead layer, i.e. copper layer in Fig. 2 of Cowles et al., because the conductive material is electrically isolated from the base layer by the

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insulating polyimide layer. As the thickness of the conductive material increases, the conductive material would inherently contact the conductive lead layer, because the conductive lead layer is in the path of the conductive material build up.

It will have been obvious to one having ordinary skill in the art to have further modified the method of Cowles et al. by electroplating the conductive material to a height equal to the surface of the conductive lead layer as taught by Rinne et al., because it would form a reliable interconnect.

Regarding claim 6, Cowles et al. differ from the instant claims in that the reference does not explicitly teach that the plated conductive material is not in contact with the conductive lead layer. However, Cowles et al. teach that solder is plated to connect the spring metal layer (i.e., stainless steel layer) to the conductive lead layer (i.e., copper layer). This creates a ground path from the copper layer to the stainless steel layer (column 3 lines 65-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. by forming a conductive material which is not in contact with the conductive lead layer if the ground path between the copper layer and the stainless steel layer is not desired. By omitting the ground path, the two layers would be electrically isolated from each other.

Regarding claim 9, Cowles et al. teach a via is opened in the ILS from the copper layer to the polyimide layer to the stainless steel layer or alternatively from the stainless steel layer to the polyimide layer to the copper layer (column 3 lines 59-62). This teaching reads on the instant claim.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowles et al. in view of Rinne et al., and further in view of Shangguan et al.

Cowles et al. and Rinne et al. teach the method as described above.

Cowles et al. differ from the instant claims in that the reference does not explicitly teach a second conductive material, i.e. gold, on the interconnect (claims 2-4); or forming a nickel layer (claim 5).

Shangguan et al. teach a method to form an interconnection between integrated circuit boards and integrated circuits. The method involves metallization of the bond pad and multiple, novel bump compositions and coating compositions to provide an interconnection which is reliable and which withstands differences in the coefficient of thermal expansion between the silicon device in the bump material (Abstract). The metalization is formed by electroplating copper over the interconnect (column 3 lines 51-56). This method is advantageous over conventional solder bumps, because it "is inexpensive, consumes a minimal amount of space, and does not require the use of wire bonding" (column 2 lines 59-63). In addition, Shangguan et al. teach depositing a nickel layer to prevent the diffusion of copper (column 4 lines 15-19), and depositing a gold layer "to provide corrosion protection for the bump during the service of the module" (column 4 lines 59-61).

Addressing claims 2-4, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al.



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by electroplating the second conductive material, such as gold, of Shangguan et al., because electroplating a gold film would provide a corrosion barrier for the interconnect.

Addressing claim 5, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. by forming the nickel film of Shangguan et al., because it would provide a diffusion barrier between the underlying conductive substrate and the copper layer.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowles et al. in view of Rinne et al., and further in view of Gay et al.

Cowles et al. teach the method as described above in addressing claim(s) 1.

The difference between the reference to Cowles et al. and the instant claims is that the reference does not explicitly teach removing oxide from the substrate before electroplating.

Gay et al. teach a method for anodic cleaning of a stainless steel substrate in order to improve to adhesion between the plated layer and the stainless steel (column 1 lines 37-43).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. and Rinne et al. by removing oxide from the substrate before electroplating as taught by Gay et al., because it would improve to adhesion between the plated layer and the stainless steel (column 1 lines 37-43 of Gay et al.).

Claims 1, 6, 7, 9-11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowles et al. in view of Rinne et al. and Young (US patent 4855871), assuming the limitation "having the physical structure of the material as electroplated" excludes solder/reflowing.

Regarding claims 1, 7, 10, 11 and 23, Cowles et al. teach a method for forming an electrical interconnect on an integrated lead suspension of the type having a spring metal layer (stainless steel layer 302, figure 2), a conductive lead layer 306 (figure 2) and an insulating layer 304 (figure 2) separating portions of the spring metal and conductive lead layers, including: forming an aperture 300 (figure 2) through at least the insulating layer and the conductive lead layer; and filling the vias with plated solder or screen solder to connect a stainless steel layer to the copper layer (column 3 lines 63-67). The solder is applied through a mask as indicated in figure 2 and removing the mask after solder 308 is formed. The plated solder forms a plated interconnect having the physical structure of the material as plated prior to reflowing.

Cowles et al. differ from the instant claims in that the reference does not explicitly teach having the physical structure of the material of the plated interconnect as electroplated; or that the conductive material initially does not electroplate onto the unmasked portions of the conductive lead layer. Cowles et al. is also silent to electroplating the conductive material to a height about equal to or greater than the surface of the conductive lead layer, although Cowles et al. teach that the plated solder achieves this height after reflowing.

Young teaches forming a thin film interconnect module utilizing a plurality of electroplated conductors in order to provide a thin film interconnect module containing a very high signal line density (column 2 lines 59-61).

Rinne et al. teach electroplating an aperture or via in the insulating layer with a conductive material to the same thickness as the top surface layer (see Fig. 1F). In addition, Rinne et al. teach using a plating base layer 24 (Fig. 1) to provide a plating current for electroplating a conductive material, i.e. solder bumps 30.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. by electroplating to form an interconnect having the physical structure of the material as electroplated as taught by Young, because it would enable the formation of a very high density interconnect (column 2 lines 59-61 of Young).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. by electroplating on the base layer, i.e. the stainless steel layer of Cowles et al., as taught by Rinne et al., because it would build up an electroplated conductive material from the bottom of the aperture, thus preventing the formation of voids. It would have been obvious to one having ordinary skill in the art to have expected that the electroplated conductive material would form on the base layer first, because an electric current is applied to the base layer to effect the electrodeposition, while the conductive material does not initially electroplate onto the conductive lead layer, i.e. copper layer in Fig. 2 of Cowles et al., because the conductive material is electrically isolated from the base layer by the

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insulating polyimide layer. As the thickness of the conductive material increases, the conductive material would inherently contact the conductive lead layer, because the conductive lead layer is in the path of the conductive material build up.

It will have been obvious to one having ordinary skill in the art to have further modified the method of Cowles et al. by electroplating the conductive material to a height equal to the surface of the conductive lead layer as taught by Rinne et al., because it would form a reliable interconnect.

Regarding claim 6, Cowles et al. differ from the instant claims in that the reference does not explicitly teach that the plated conductive material is not in contact with the conductive lead layer. However, Cowles et al. teach that solder is plated to connect the spring metal layer (i.e., stainless steel layer) to the conductive lead layer (i.e., copper layer). This creates a ground path from the copper layer to the stainless steel layer (column 3 lines 65-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. by forming a conductive material which is not in contact with the conductive lead layer if the ground path between the copper layer and the stainless steel layer is not desired. By omitting the ground path, the two layers would be electrically isolated from each other.

Regarding claim 9, Cowles et al. teach a via is opened in the ILS from the copper layer to the polyimide layer to the stainless steel layer or alternatively from the stainless steel layer to the polyimide layer to the copper layer (column 3 lines 59-62). This teaching reads on the instant claim.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowles et al. in view of Rinne et al. and Young, and further in view of Shangguan et al.

Cowles et al., Rinne et al. and Young teach the method as described above. The basis of rejection of the instant claims parallel that given above.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowles et al. in view of Rinne et al. and Young, and further in view of Gay et al.

Cowles et al., Rinne et al. and Young teach the method as described above. The basis of rejection of the instant claims parallel that given above.

### ***Response to Arguments***

In the arguments presented on page 9 of the amendment, the applicant argues that the process of the instant invention as claimed in the amendment is considerably different than that taught or suggested by Cowles et al. and Rinne et al.; specifically Cowles et al. teach that the solder is initially plated onto the exposed surfaces of both the stainless steel and copper layers in the via. The examiner acknowledges that the latter statement is correct. However, the solder is initially plated on both the stainless steel and copper layers in the via in order to increase the amount of solder being plated. Since the plated solder is subsequently reflowed in the via, the solder would be evenly distributed within the via to form the interconnect. Therefore, because solder is plated and reflowed, plating on either one of the layers or both layers simultaneously does not

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affect the final interconnect. If the interconnect is electroplated without solder/reflow, as taught by Young, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Cowles et al. by electroplating on the base layer, i.e. the stainless steel layer of Cowles et al., as taught by Rinne et al., because it would build up an electroplated conductive material from the bottom of the aperture, thus preventing the formation of voids.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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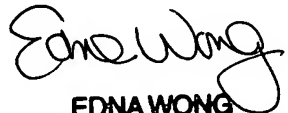
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan V. Van whose telephone number is 571-272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LVV

May 30, 2007

  
EDNA WONG  
PRIMARY EXAMINER  
6/1/07